IN THE CLAIMS:

Please amend the claims as set forth below:

1-20. (Cancelled)

21. (New) A conditional clock buffer circuit having a clock output and coupled to receive a clock input and a condition signal, the conditional clock buffer circuit comprising:

a first circuit coupled to receive the clock input and coupled to a first node within the conditional clock buffer circuit, the first circuit configured to generate a first state on the first node responsive to a first phase of the clock input;

a second circuit coupled to receive the clock input and the condition signal and coupled to the first node, wherein the second circuit is configured to conditionally generate a second state on the first node during a condition window within a second phase of the clock input, wherein the condition window excludes at least a portion of the second phase, and wherein the second circuit is configured to conditionally generate the third state responsive to the condition signal during the condition window; and

a third circuit coupled to the first node and to the clock output, the third circuit configured to generate a third state on the clock output responsive to the first state on the first node and configured to generate a fourth state on the clock output responsive to the second state on the first node.

22. (New) The conditional clock buffer circuit as recited in claim 21 wherein the second circuit is further configured to prevent charge sharing between the first node and a second node within the second circuit if the condition signal indicates that the second state is not to be generated on the clock output during the condition window.

23. (New) The conditional clock buffer circuit as recited in claim 22 wherein the second circuit comprises a first transistor coupled to the second node and having a first control node coupled to the condition signal, the first transistor charging the second node in response to the condition signal indicating that the second state is not to be generated on the clock output.

24. (New) The conditional clock buffer circuit as recited in claim 22 wherein the second circuit comprises a plurality of transistors coupled in series, wherein a first transistor of the plurality of transistors has a first control node that is coupled to receive the clock input and a second transistor of the plurality of transistors has a second control node that is coupled to receive the condition signal, and wherein the second node is a node between the first transistor and the second transistor.

25. (New) The conditional clock buffer circuit as recited in claim 24 wherein the second circuit further comprises a third transistor coupled to the second node and having a third control node coupled to the condition signal, the third transistor charging the node in response to the condition signal indicating that the second state is not to be generated on the clock output.

26. (New) The conditional clock buffer circuit as recited in claim 24 wherein the plurality of transistors further comprises a third transistor having a third control node that is coupled to receive an inverse of the clock input with a delay.

27. (New) The conditional clock buffer circuit as recited in claim 26 wherein the delay defines a width of the condition window.

28. (New) The conditional clock buffer circuit as recited in claim 26 wherein the inverse of the clock input is generated by a logic gate coupled to receive the clock input and having an output coupled to the third control node.

29. (New) The conditional clock buffer circuit as recited in claim 28 wherein the logic

gate is sized to generate the delay of about 1/4 of the second phase.

30. (New) The conditional clock buffer circuit as recited in claim 28 wherein the logic gate is sized to generate the delay of about 2 gate delays.

31. (New) The conditional clock buffer circuit as recited in claim 28 wherein the logic gate is an inverter.

32. (New) The conditional clock buffer circuit as recited in claim 21 wherein the third circuit comprises a latch circuit configured to hold the clock output during the portion of the second phase that is excluded from the condition window.

33. (New) The conditional clock buffer circuit as recited in claim 21 wherein the condition window is about 1/4 of the second phase.

34. (New) The conditional clock buffer circuit as recited in claim 21 wherein the condition window is about 2 gate delays.

35. (New) A clock tree comprising:

one or more levels of buffering coupled to receive an input clock and output a buffered clock; and

a plurality of conditional clock buffer circuits coupled to receive the buffered clock and a condition signal, at least some of the conditional clock buffer circuits receiving different condition signals than other ones of the conditional clock buffer circuits, each conditional clock buffer circuit having a clock output and including:

a first circuit coupled to receive the buffered clock and coupled to a first node within the conditional clock buffer circuit, the first circuit

configured to generate a first state on the first node responsive to a first phase of the buffered clock;

a second circuit coupled to receive the buffered clock and the condition signal and coupled to the first node, wherein the second circuit is configured to conditionally generate a second state on the first node during a condition window within a second phase of the buffered clock, wherein the condition window excludes at least a portion of the second phase, and wherein the second circuit is configured to conditionally generate the third state responsive to the condition signal during the condition window; and

a third circuit coupled to the first node and to the clock output, the third circuit configured to generate a third state on the clock output responsive to the first state on the first node and configured to generate a fourth state on the clock output responsive to the second state on the first node.

36. (New) The clock tree as recited in claim 35 wherein the second circuit of each conditional clock buffer circuit is further configured to prevent charge sharing between the first node and a second node within the second circuit if the condition signal indicates that the second state is not to be generated on the clock output during the condition window.

37. (New) The clock tree as recited in claim 36 wherein the second circuit comprises a first transistor coupled to the second node and having a first control node coupled to the condition signal, the first transistor charging the second node in response to the condition signal indicating that the second state is not to be generated on the clock output.

38. (New) The clock tree as recited in claim 36 wherein the second circuit comprises a plurality of transistors coupled in series, wherein a first transistor of the plurality of

transistors has a first control node that is coupled to receive the buffered clock and a second transistor of the plurality of transistors has a second control node that is coupled to receive the condition signal, and wherein the second node is a node between the first transistor and the second transistor.

39. (New) The clock tree as recited in claim 35 wherein the third circuit comprises a latch circuit configured to hold the clock output during the portion of the second phase that is excluded from the condition window.

40. (New) The clock tree as recited in claim 35 wherein the condition window is about 1/4 of the second phase.

41. (New) The clock tree as recited in claim 35 wherein the condition window is about 2 gate delays.

42. (New) A computer accessible medium comprising one or more data structures which are operated upon by a program executable on a computer system, the program operating on the data structures to perform a portion of a process to fabricate an integrated circuit including circuitry described by the data structures, the circuitry described in the data structures including a conditional clock buffer circuit having a clock output and coupled to receive a clock input and a condition signal, the conditional clock buffer circuit comprising:

a first circuit coupled to receive the clock input and coupled to a first node within the conditional clock buffer circuit, the first circuit configured to generate a first state on the first node responsive to a first phase of the clock input;

a second circuit coupled to receive the clock input and the condition signal and coupled to the first node, wherein the second circuit is configured to conditionally generate a second state on the first node during a condition window within a second phase of the clock input, wherein the condition

window excludes at least a portion of the second phase, and wherein the second circuit is configured to conditionally generate the third state responsive to the condition signal during the condition window; and

a third circuit coupled to the first node and to the clock output, the third circuit configured to generate a third state on the clock output responsive to the first state on the first node and configured to generate a fourth state on the clock output responsive to the second state on the first node.